Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (currently amended) A bus interface converter capable of converting AMBA AHB bus protocol into i960-like bus protocol, ~~characterized in that~~ wherein the converter comprising:

an AHB interface for accomplishing interface processing for AMBA AHB bus protocol;

an i960-like interface for accomplishing interface processing for i960-like bus protocol; and

a main controller for accomplishing bus protocol conversion between the AHB interface and the i960-like interface;

wherein, the AHB interface comprising:

an AHB bus signal register module for accomplishing judgment and register for control signal from an AMBA AHB bus;and

an AHB bus signal response module for generaing corresponding response indicating signal of AMBA AHB bus protocol;

the i960-like interface comprising:

a bus interface multiplexing request module for generating bus interface multiplexing request signal; and

a bus multiplexing module for accomplishing the multiplexing between the address bus for outputting from AHB to i960-like and the data bus for outputting from AHB to i960-like.

2. (currently amended) The converter according to Claim 1, ~~characterized in that~~ wherein the AHB bus signal register module further comprises:

an AHB bus write buffer module for performing buffering to the write data and write address from AHB bus.

3. (currently amended)The converter according to Claim 2, ~~characterized in that~~ wherein the AHB bus write buffer module comprises two buffering fields: address field and data field.

4. (currently amended) The converter according to Claim 2, ~~characterized in that~~ wherein the AHB bus write buffer module has an enabling port, and can set the size of buffering fields for the address field and data field of the AHB bus write buffer module via AHB bus.

5. (currently amended) The converter according to Claim 1, ~~characterized in that~~ wherein the AHB bus signal response module serves to generate AMBA AHB bus feedback signals HREADYout and HRESP.

6. (currently amended) The converter according to Claim 1, ~~characterized in that~~ wherein the i960-like interface has the request and response function of accessing outside shared bus, which can be connected to a bus interface multiplexing controller and then connected to i960-like bus after bus multiplexing.

7. (currently amended) The converter according to Claim 1, ~~characterized in that~~ wherein the i960-like interface can be directly connected to i960-like bus.

8. (currently amended) The converter according to Claim 1, ~~characterized in that~~ wherein the bus interface multiplexing request module determines whether to send bus request signal to the bus interface unit based on the state indicating signal from the main controller, and determines whether to stop sending bus request signal to the bus interface multiplexing controller based on response signal from i960-like bus.

9. (currently amended) The converter according to Claim 1, ~~characterized in that~~ wherein the address and data multiplexing output bus of the bus multiplexing module is connected to the top interconnected logic module, and multiplexed with ADS-IN signal into a tri-state dual-direction address data bus signal through tri-state gate.

10. (currently amended) The converter according to Claim 1, ~~characterized in that~~ wherein the main controller has two clocks being synchronous with AHB bus clock and i960-like bus clock respectively.

11. (currently amended) The converter according to Claim 1, ~~characterized in that~~ wherein the clock frequency of the AHB bus may be N times of that of the i960-like bus, where N is a natural number no less than 1.

12. (currently amended) The converter according to Claim 1, ~~characterized in that~~ wherein the main controller has a state machine, which serves to indicate the current state of the main controller, and the state machine has three states: idle, read and write.

13. (currently amended) The converter according to Claim 1, ~~characterized in that~~ wherein the clock of the i960-like interface can be set to be in normal mode or low-power mode, in the low-power mode, the i960-like interface clock is dynamatically controlled

by the bus request signal sent by the bus interface multiplexing request module, when there is communication betweem AHB bus and i960-like bus, the clock of i960-like interface is valid, and when there is no communication between AHB bus and i960-like bus, the bus clock of the i960-like interface is set high to suspend.